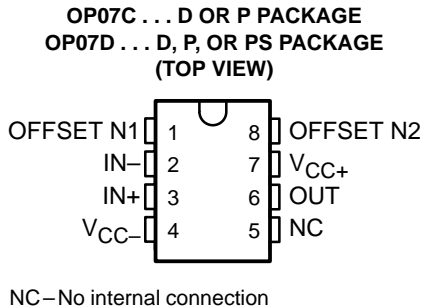


- **Low Noise**
- **No External Components Required**
- **Replace Chopper Amplifiers at a Lower Cost**
- **Wide Input-Voltage Range**
... 0 to ± 14 V Typ
- **Wide Supply-Voltage Range**
... ± 3 V to ± 18 V
- **Essentially Equivalent to Fairchild μ A714 Operational Amplifiers**
- **Direct Replacements for PMI OP07C and OP07D**



description

These devices offer low offset and long-term stability by means of a low-noise, chopperless, bipolar-input-transistor amplifier circuit. For most applications, external components are not required for offset nulling and frequency compensation. The true differential input, with a wide input-voltage range and outstanding common-mode rejection, provides maximum flexibility and performance in high-noise environments and in noninverting applications. Low bias currents and extremely high input impedances are maintained over the entire temperature range. The OP07 is unsurpassed for low-noise, high-accuracy amplification of very-low-level signals.

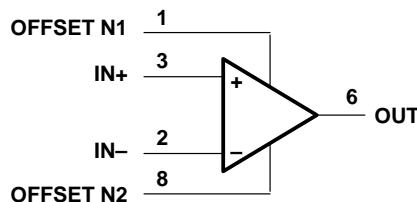
These devices are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T _A	V _{IO} MAX AT 25°C	PACKAGE	
		SMALL OUTLINE (D, PS)	PLASTIC DIP (P)
0°C to 70°C	150 μ V	OP07CD	OP07CP
		OP07DD OP07DPS	OP07DP

The D package is available taped and reeled. Add the suffix R to the device type (e.g., OP07CDR). The PS package is available only taped and reeled.

symbol

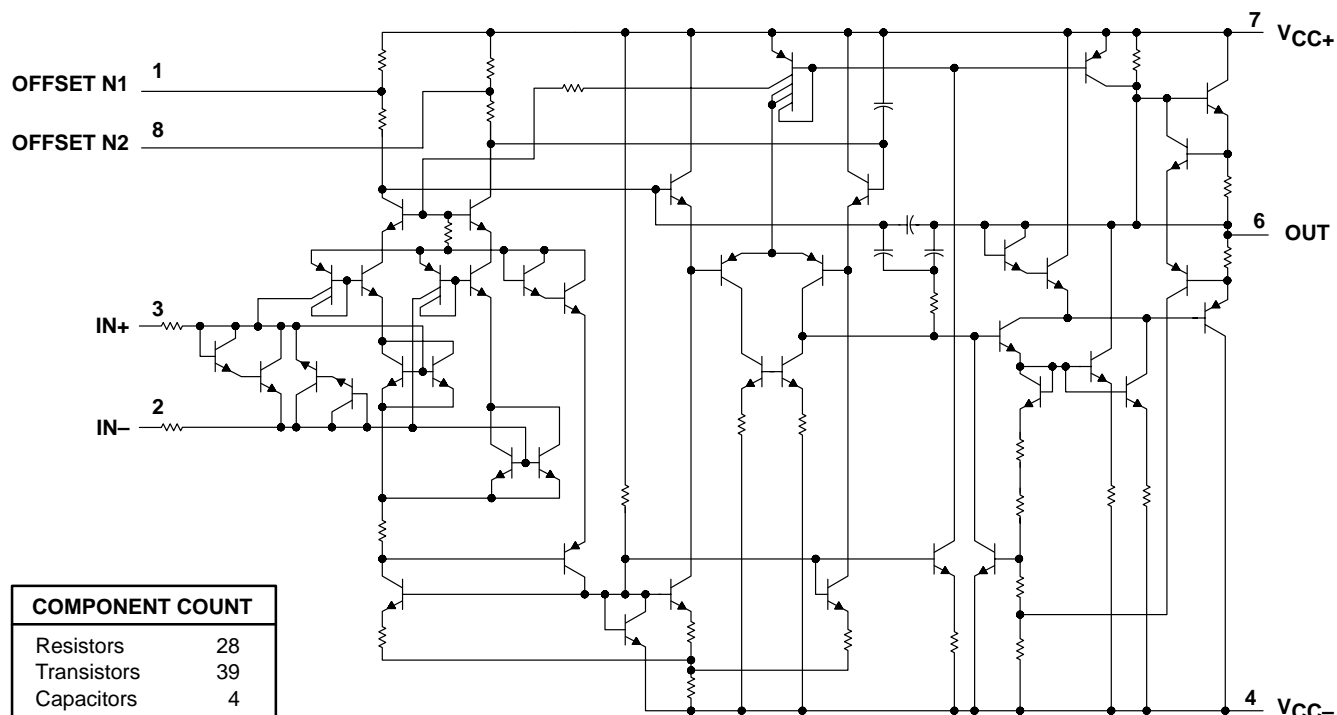


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OP07C, OP07D PRECISION OPERATIONAL AMPLIFIERS

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schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage: V_{CC+} (see Note 1)	22 V
V_{CC-} (see Note 1)	-22 V
Differential input voltage (see Note 2)	± 30 V
Input voltage, V_I (either input, see Note 3)	± 22 V
Duration of output short circuit (see Note 4)	Unlimited
Package thermal impedance, θ_{JA} (see Note 5): D package	97°C/W
P package	85°C/W
PS package	95°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-} .

2. Differential voltages are at $IN+$ with respect to $IN-$.

3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.

4. The output may be shorted to ground or either power supply.

5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	MAX	UNIT
$V_{CC\pm}$	Supply voltage	± 3	± 18	V
V_{IC}	Common-mode input voltage	-13	13	V
T_A	Operating free-air temperature	0	70	°C



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electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	T _A	OP07C			OP07D			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO} Input offset voltage	V _O = 0, R _S = 50 Ω	25°C		60	150		60	150	μV
		0°C to 70°C		85	250		85	250	
α _{VIO} Temperature coefficient of input offset voltage	V _O = 0, R _S = 50 Ω	0°C to 70°C		0.5	1.8		0.7	2.5	μV/°C
Long-term drift of input offset voltage	See Note 6			0.4			0.5		μV/mo
Offset adjustment range	R _S = 20 kΩ, See Figure 1	25°C		±4			±4		mV
I _{IO} Input offset current		25°C		0.8	6		0.8	6	nA
		0°C to 70°C		1.6	8		1.6	8	
α _{IIO} Temperature coefficient of input offset current		0°C to 70°C		12	50		12	50	pA/°C
I _{IB} Input bias current		25°C		±1.8	±7		±2	±12	nA
		0°C to 70°C		±2.2	±9		±3	±14	
α _{IIB} Temperature coefficient of input bias current		0°C to 70°C		18	50		18	50	pA/°C
V _{ICR} Common-mode input voltage range		25°C		±13	±14		±13	±14	V
		0°C to 70°C		±13	±13.5		±13	±13.5	
V _{OM} Peak output voltage	R _L ≥ 10 kΩ	25°C		±12	±13		±12	±13	V
	R _L ≥ 2 kΩ			±11.5	±12.8		±11.5	±12.8	
	R _L ≥ 1 kΩ				±12			±12	
	R _L ≥ 2 kΩ		0°C to 70°C		±11	±12.6		±11	
A _{VD} Large-signal differential voltage amplification	V _{CC±} = ±3 V, V _O = ±0.5 V, R _L ≥ 500 kΩ	25°C		100	400		400		V/mV
	V _O = ±10 V, R _L = 2 kΩ	25°C		120	400		120	400	
		0°C to 70°C		100	400		100	400	
B ₁ Unity-gain bandwidth		25°C		0.4	0.6		0.4	0.6	MHz
r _i Input resistance		25°C		8	33		7	31	MΩ
CMRR Common-mode rejection ratio	V _{IC} = ±13 V, R _S = 50 Ω	25°C		100	120		94	110	dB
		0°C to 70°C		97	120		94	106	
k _{SVS} Supply-voltage sensitivity (ΔV _{IO} /ΔV _{CC})	V _{CC±} = ±3 V to ±18 V, R _S = 50 Ω	25°C		7	32		7	32	μV/V
		0°C to 70°C		10	51		10	51	
P _D Power dissipation	V _O = 0, No load	25°C		80	150		80	150	mW
	V _{CC±} = ±3 V, V _O = 0, No load			4	8		4	8	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise noted.

NOTE 6: Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a warranty. It is an engineering estimate of the averaged trend line of drift versus time over extended periods after the first thirty days of operation.

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operating characteristics, $V_{CC\pm} = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS†	OP07C	OP07D	UNIT
		TYP	TYP	
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$	10.5	10.5	$\text{nV}/\sqrt{\text{Hz}}$
	$f = 100\text{ Hz}$	10.2	10.3	
	$f = 1\text{ kHz}$	9.8	9.8	
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }10\text{ Hz}$	0.38	0.38	μV
I_n Equivalent input noise current	$f = 10\text{ Hz}$	0.35	0.35	$\text{pA}/\sqrt{\text{Hz}}$
	$f = 100\text{ Hz}$	0.15	0.15	
	$f = 1\text{ kHz}$	0.13	0.13	
$I_{N(PP)}$ Peak-to-peak equivalent input noise current	$f = 0.1\text{ Hz to }10\text{ Hz}$	15	15	pA
SR Slew rate	$R_L \geq 2\text{ k}\Omega$	0.3	0.3	$\text{V}/\mu\text{s}$

† All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise noted.

APPLICATION INFORMATION

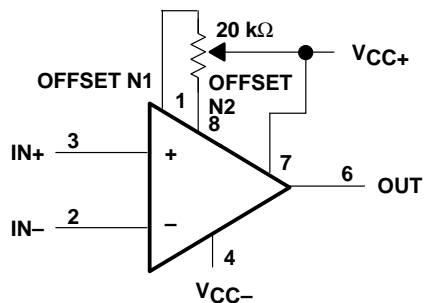


Figure 1. Input Offset-Voltage Null Circuit

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